REMARKS

The claims are claims 1, 2, 4 and 7 to 11.

The application has been amended at many locations to correct minor errors and to present uniform language throughout. The amendments include correction of those errors noted by the Examiner. These amendments include insertion of reference numbers originally omitted from the text.

A new set of formal drawings including drawing corrections is attached. The new drawings include the label "EXTERNAL PERIPHERALS" within box 82 of Figure 2 and change "Fig. 7A" to "Fig. 7B" as required by the Examiner. The reference number "10/40" appearing in Figure 11 has not been changed as requested by the Examiner. Instead, the text at page 29 to indicate that central processing unit 10 and integrated circuit 40 are co-located. By this change in the text, Figure 11 is correct.

Claims 1, 4 and 7 are amended. Claims 3, 5 and 6 are canceled. New claims 8 to 11 are added. Claims 1, 4 and 7 are amended to distinguish over the cited reference. New claims 8 and 9 correspond to claims 2 and 4 except dependent upon method claim 7. Claims 10 and 11 are respective apparatus and method claims reciting a limitation on execute packets upon a branch.

Claims 1, 2, 4 and 7 were rejected under 35 U.S.C. 102(e) as being anticipated by Sharangpani et al., U.S. Patent No. 6,237,077.

Claims 1 and 7 recite subject matter not anticipated by Sharangpani et al. Claim 1 recites each instruction includes "a predetermined p-bit, said p-bit having a first digital state indicating a next instruction is to execute in parallel with said instruction and a second digital state indicating a next instruction is to execute in a cycle after said instruction" and that the dispatch circuitry selects an execution packet "by scanning instructions from lower memory address locations to higher

memory address locations adding an instruction to said execute packet when said p-bit of a prior instruction has said first digital state until said p-bit of an instruction has said second digital state." Claim 7 recites each instruction includes a predetermined p-bit, said p-bit having a first digital state indicating a next instruction is to execute in parallel with said instruction and a second digital state indicating a next instruction is to execute in a cycle after said instruction" and "scanning the p-bit of each instruction of each fetch packet from lowest memory address location to highest memory address location to determine an execute packet dependent upon the p-bits." Claims 1 and 7 recite coding of the execute packets in a different manner than disclosed in Sharangpani et al. Sharangpani et al teaches template field 220 marks any instruction group boundary within an instruction bundle and stop field 230 whether an instruction group boundary is at the instruction bundle boundary. Sharangpani et al states at column 4, line 64 to column 5, line 7:

> "Template field 220 encodes the position of any instruction group boundaries within instruction bundle 200, as well as a template type that indicates how instruction slots 210 are mapped to execution units. Here, an instruction group boundary identifies the last instruction in an instruction group as defined above. Stop field 230 indicates when an instruction group boundary coincides with the last instruction slot of bundle 200. Thus, template field 220 specifies the configuration of instructions within bundle 200, and with stop field 230, indicates the boundaries between adjacent instruction groups."

In contrast, the recitations of claims 1 and 7 employ the p-bit to mark both execute packet boundaries within a fetch packet and at a fetch packet boundary. Accordingly, claims 1 and 7 are not anticipated by Sharangpani et al.

Claims 1 and 7 recite further subject matter not anticipated by Sharangpani et al. Claim 1 recites "each instruction including

an instruction type" and the dispatch circuitry operates to "dispatch each instruction of said selected execute packet to a functional unit corresponding to said instruction type of said instruction." Claim 7 recites "each instruction including an instruction type" and "dispatching each instruction within the determined execute packet to one of a second plurality of execution units dependent upon an instruction type of the instruction." Thus the mapping of instructions within a fetch packet to functional unit differs from Sharangpani et al. As quoted above, Sharangpani et al states that template field 220 "indicates how instruction slots 210 are mapped to execution units." This differs from the recitations of claims 1 and 7. Thus, claims 1 and 7 are not anticipated by Sharangpani et al.

Claim 2 recites subject matter not anticipated by Sharangpani et al. Claim 2 recites "the first plurality is equal in number to the second plurality," that is the number of instructions in a fetch packet is the same as the number of functional units. The OFFICE ACTION cites Figure 3 and column 7, lines 25 to 32 of Sharangpani et al as anticipating this subject matter. Sharangpani et al teaches at column 4, lines 54 to 57 and illustrates at Figure 2 that each instruction bundle 200 includes three instructions. Sharangpani et al teaches at column 7, lines 25 to 32 that three branch execution units enables execution of three branch instructions. However, Figure 3 of Sharangpani et al clearly illustrates two memory execution units M0 and M1, two integer execution units Io and I1 and two floating point execution units F0 and F1. Thus Figure 3 of Sharangpani et al illustrates 9 execution units. This does not equal the three instructions per instruction bundle illustrated in Figure 2 as required by the recitations of claim 2. Accordingly, claim 2 is not anticipated by Sharangpani et al.

Claim 4 recites subject matter not anticipated by Sharangpani et al. Claim 4 recites "a first plurality of multiplexers, each multiplexer having a first input receiving an instruction from a predetermined position of said first latch, a second input receiving an instruction from a corresponding position of said second latch, a control input and an output, each multiplexer selecting at said output said instruction from said first latch, said instruction from said second latch or no instruction dependent upon said control input." Sharangpani et al fails to teach these multiplexers. Thus claim 4 is not anticipated by Sharangpani et al.

New claim 8 is a method claim reciting subject matter similar to apparatus claim 2 and is likewise allowable.

New claim 9 is a method claim reciting subject matter similar to apparatus claim 4 and is likewise allowable.

New claims 10 and 11 recite subject matter not anticipated by Sharangpani et al. Claims 10 and 11 recite the dispatch circuitry operates to select an execution packet "wherein upon a branch into the middle of an execute packet not selecting instructions having memory address locations lower than the branch." The Applicants respectfully submit that Sharangpani et al includes no disclosure of this subject matter. Accordingly, claims 10 and 11 are allowable.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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